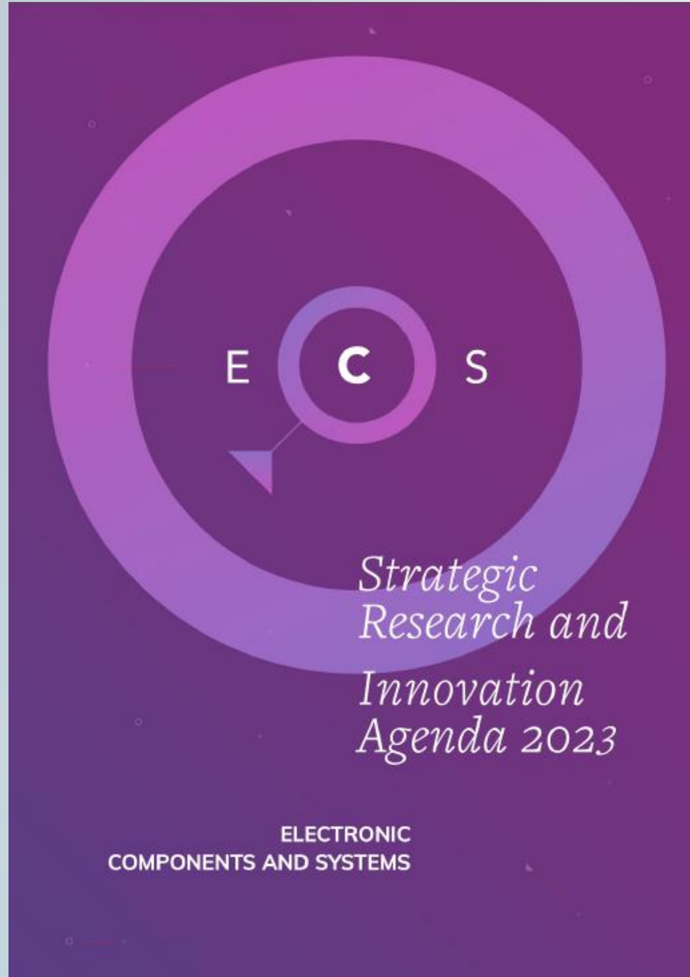
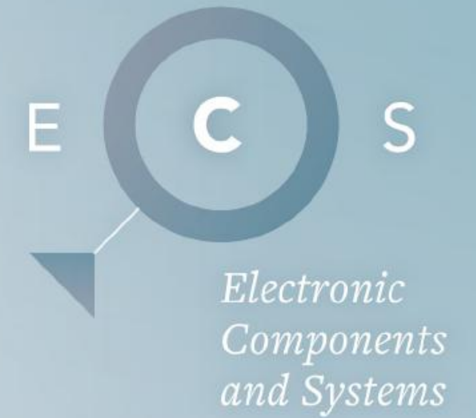
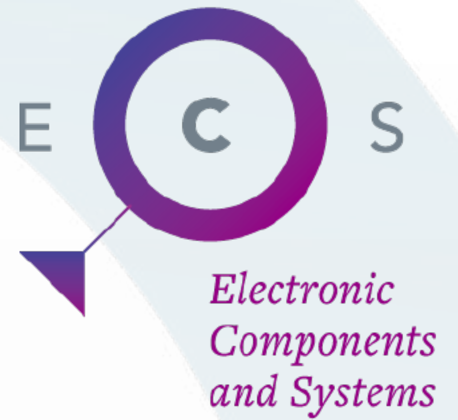




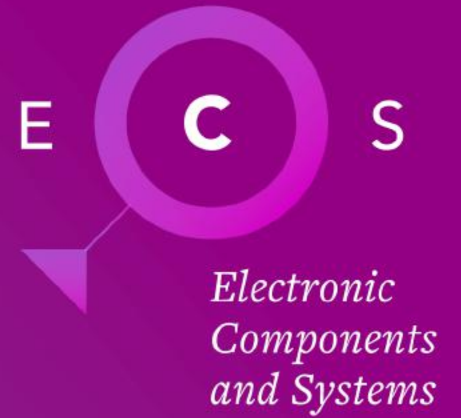
ECS-SRIA 2023 & KDT Calls Guide

Paolo Azzoni
ECS-SRIA Chairman
Inside Industry Association

Summary

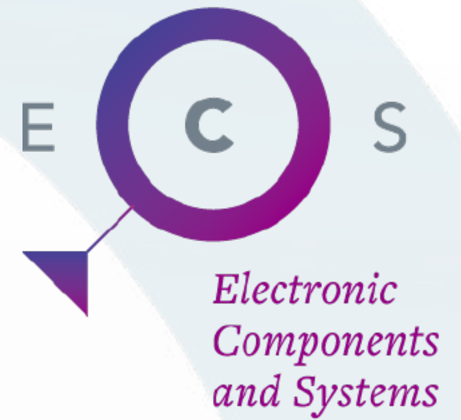


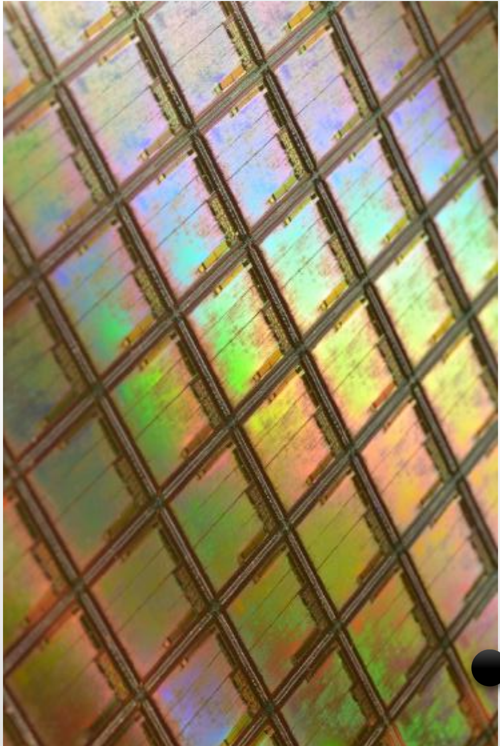
- Introduction
- The new ECS-SRIA web site
- ECS-SRIA 2023 & Focus Topics
- ECS-SRIA 2023 updates (for reference)



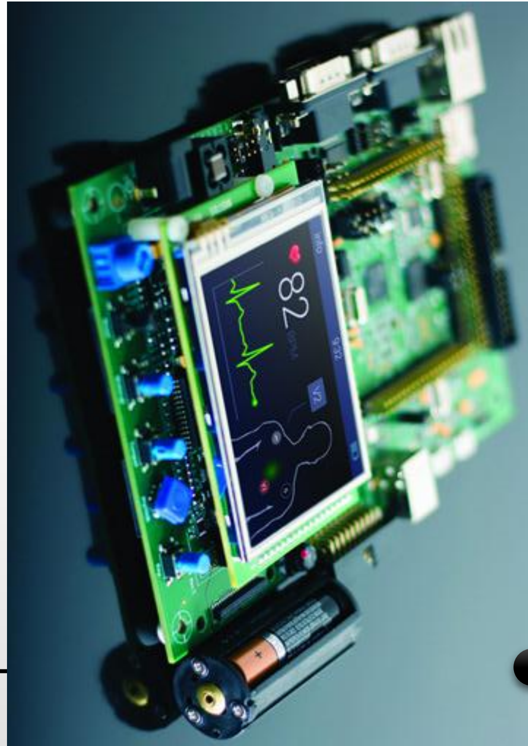
The ECS-SRIA and its role

The SRIA for the ECS value chain

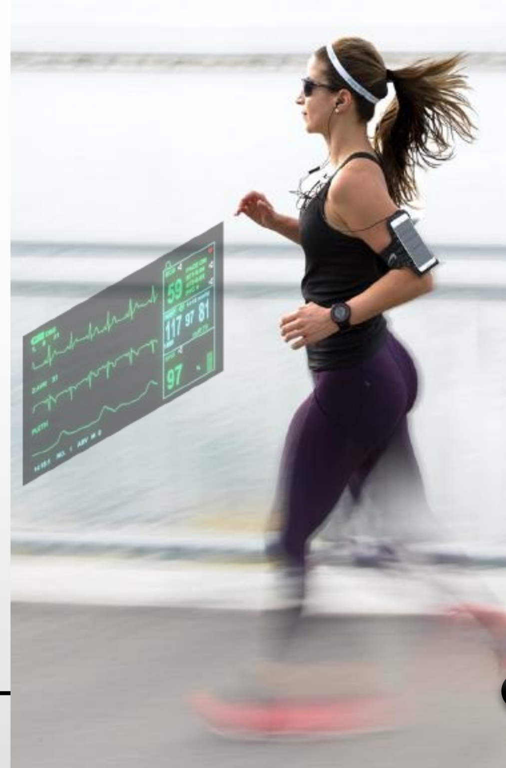




Materials, processes, semiconductors, micro & nano electronic components, ...



Smart sensors, integrated devices, edge AI, embedded SW, ...

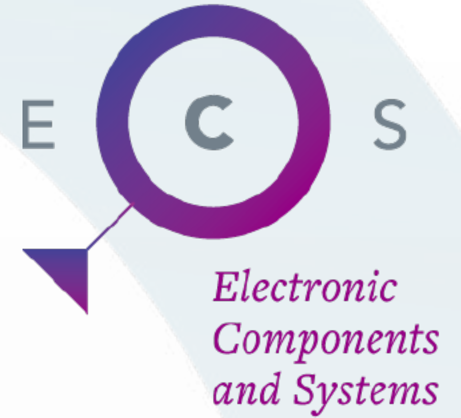


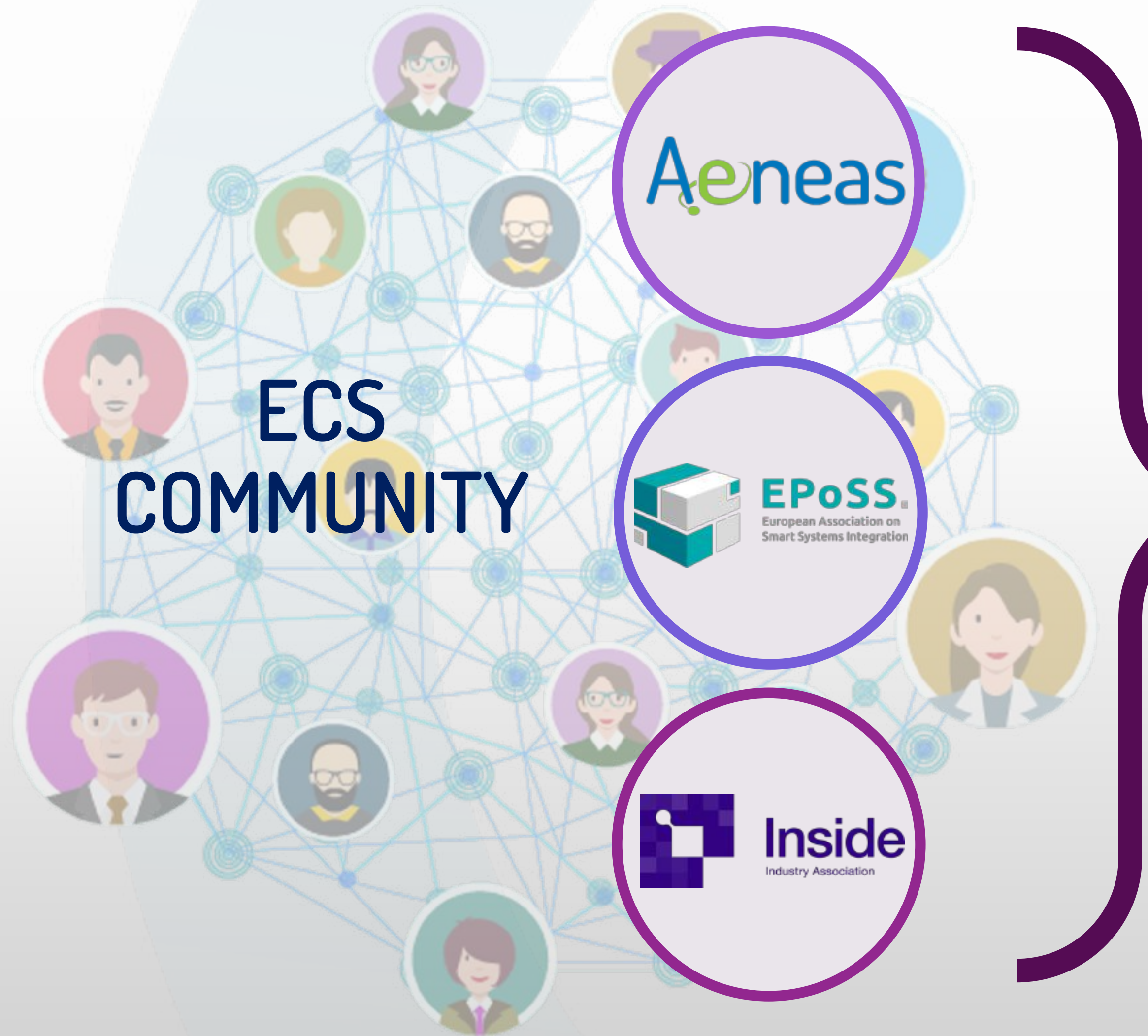
Systems and applications, value creation, societal goals, ...

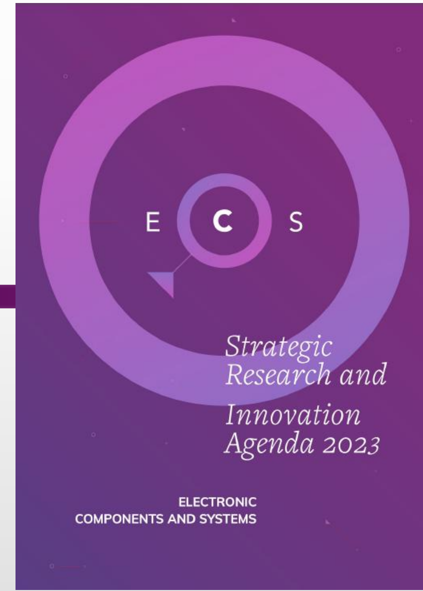
ECS engineering tools

The ECS-SRIA 2023

Basis for KDT Calls 2023





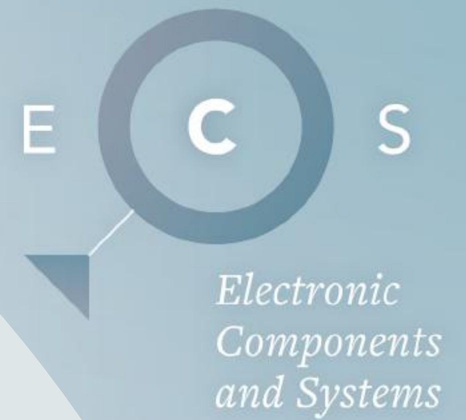


Paolo Azzoni
Inside IA
Chairman

Patrick Cogez
AENEAS
Co-chairman

Nicolas Gouze
EPOSS
Co-chairman

The ECS-SRIA Team 2023



Core Team

- Arco Krijgsman - ASML
- Christophe Wyon - CEA
- Jerker Delsing - LTU
- Juergen Niehaus - Safetrans
- Patrick Pype - NXP
- Sven Rzepka - Fraunhofer
- Wolfgang Dettmann - Infineon

More than 300 European experts

ECS-SRIA structure

Basic technology stack of a typical digitalization solution & hierarchical dependencies

Key ECS application domains for Europe
Enabled by and driving ECS technology roadmaps

1 FOUNDATIONAL TECHNOLOGY LAYERS
- 1.4 System of Systems
- 1.3 Embedded Software and Beyond
- 1.2 Components, Modules and Systems Integration
- 1.1 Process Technology, Equipment, Materials and Manufacturing

2 CROSS-SECTIONAL TECHNOLOGIES
- 2.1 Edge Computing and Embedded Artificial Intelligence
- 2.2 Connectivity
- 2.3 Architecture and Design: Methods and Tools
- 2.4 Quality, Reliability, Safety and Cybersecurity

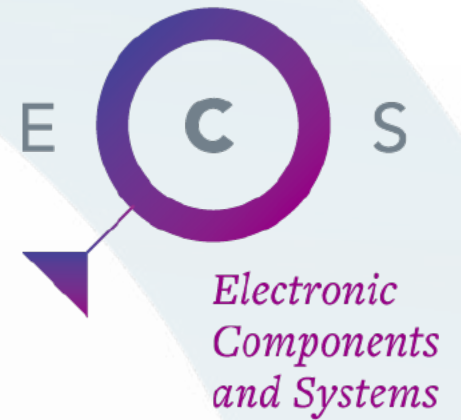
3 ECS KEY APPLICATION AREAS
- 3.1 Mobility
- 3.2 Energy
- 3.3 Digital Industry
- 3.4 Health and Wellbeing
- 3.5 Agrifood and Natural Resources
- 3.6 Digital Society

4 LONG TERM VISION

What needs to be addressed now at low TRL level to feed the innovation pipeline

Transversal areas
- Benefiting from interdisciplinary contribution of the foundational layers
- Or supporting technology stack across all layers

ECS SRIA and KDT calls 2023



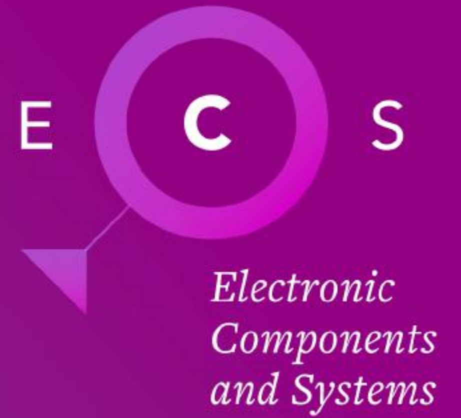
Basis for KDT calls 2023

Global Call:

- Includes all Major Challenges of the SRIA (from CHP 1.1 to 3.6)
- Refer directly to the ECS-SRIA for both RIA and IA

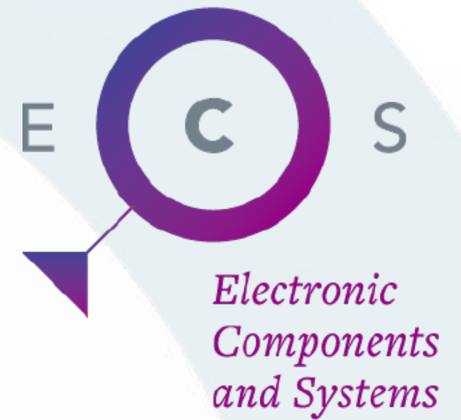
Focus Topics:

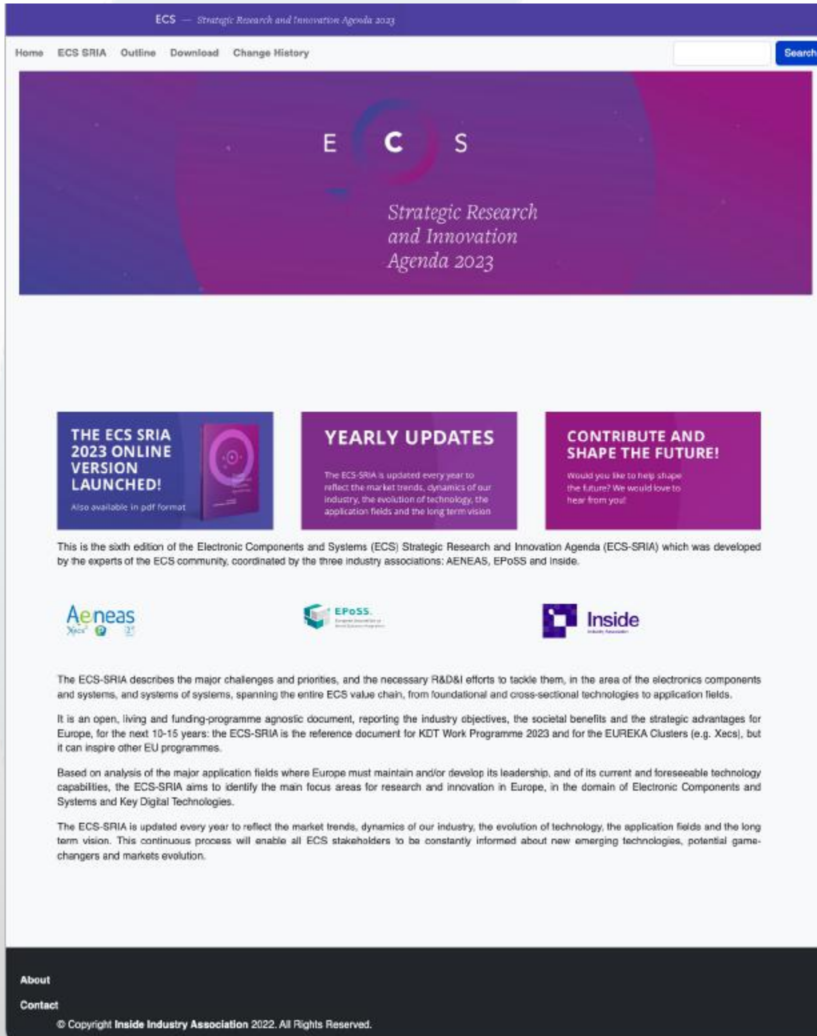
- Refer to call text
- ECS-SRIA is aligned with focus topics
- The ECS-SRIA represents a complementary source of information to:
  - position the focus topics in the ECS value chain
  - identify synergies/dependencies with other technology areas (interdisciplinarity)



ECS-SRIA Web Site

ECS-SRIA Web Site



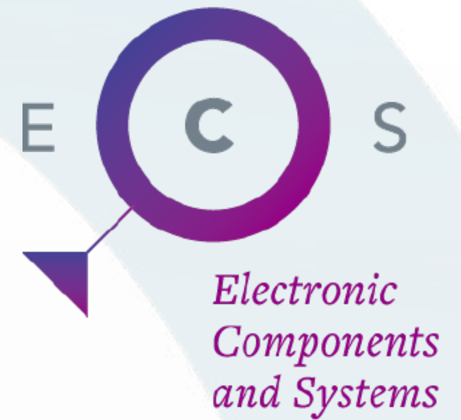


The ECS-SRIA goes online!

- Increased visibility and accessibility
- Simple to browse with hyperlinks
- Attract new talents and experts
- Native indexing and analytics
- More advanced functionalities for:
  - Topics search
  - Selective reading
- W3C standard

The SRIA outline

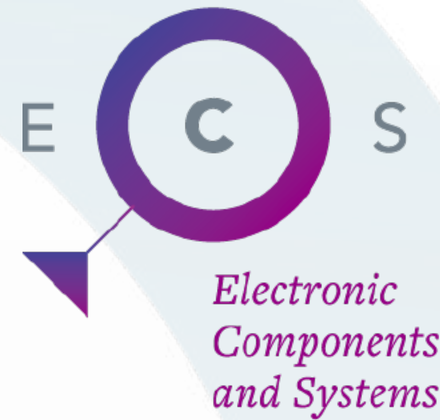
The outline is the landing page for beginners!



Summary of the Chapter scope

Clarifies the role of the chapters, the technology domains they cover and the synergies between them, simplifying the comprehension of the ECS-SRIA and its “navigation”.

The SRIA outline (2)



ECS — Strategic Research and Innovation Agenda 2023

Home ECSSRIA Outline ECS SRIA Contributors Download Change History Search

CROSS-SECTIONAL TECHNOLOGIES

2.1 - EDGE COMPUTING AND EMBEDDED ARTIFICIAL INTELLIGENCE

2.2 - CONNECTIVITY

2.3 - ARCHITECTURE AND DESIGN: METHODS AND TOOLS

2.4 - QUALITY, RELIABILITY, SAFETY AND CYBERSECURITY

FOUNDATIONAL TECHNOLOGY LAYERS

1.4 - SYSTEM OF SYSTEMS

1.3 - EMBEDDED SOFTWARE AND BEYOND

1.2 - COMPONENTS, MODULES AND SYSTEMS INTEGRATION

1.1 - PROCESS TECHNOLOGY, EQUIPMENT, MATERIALS AND MANUFACTURIN

Click on the buttons for more information

SYNERGIES BETWEEN 1.2 AND 2.4

Growing complexity of smart components, modules and systems represents a reliability challenge which requires the continuous improvement of existing methods (e.g. design for reliability) and development of new techniques (e.g. prognostic health management) for reliable ECS. The area also focuses on solutions for ensuring secure integration of systems, sensor level hardware and software security, privacy and data trustworthiness and AI Hardware safety.

Synergies between chapters

The “matrix” highlights synergies, dependencies and links between chapters: the SRIA is highly interdisciplinary

Global Timelines
Short-term example

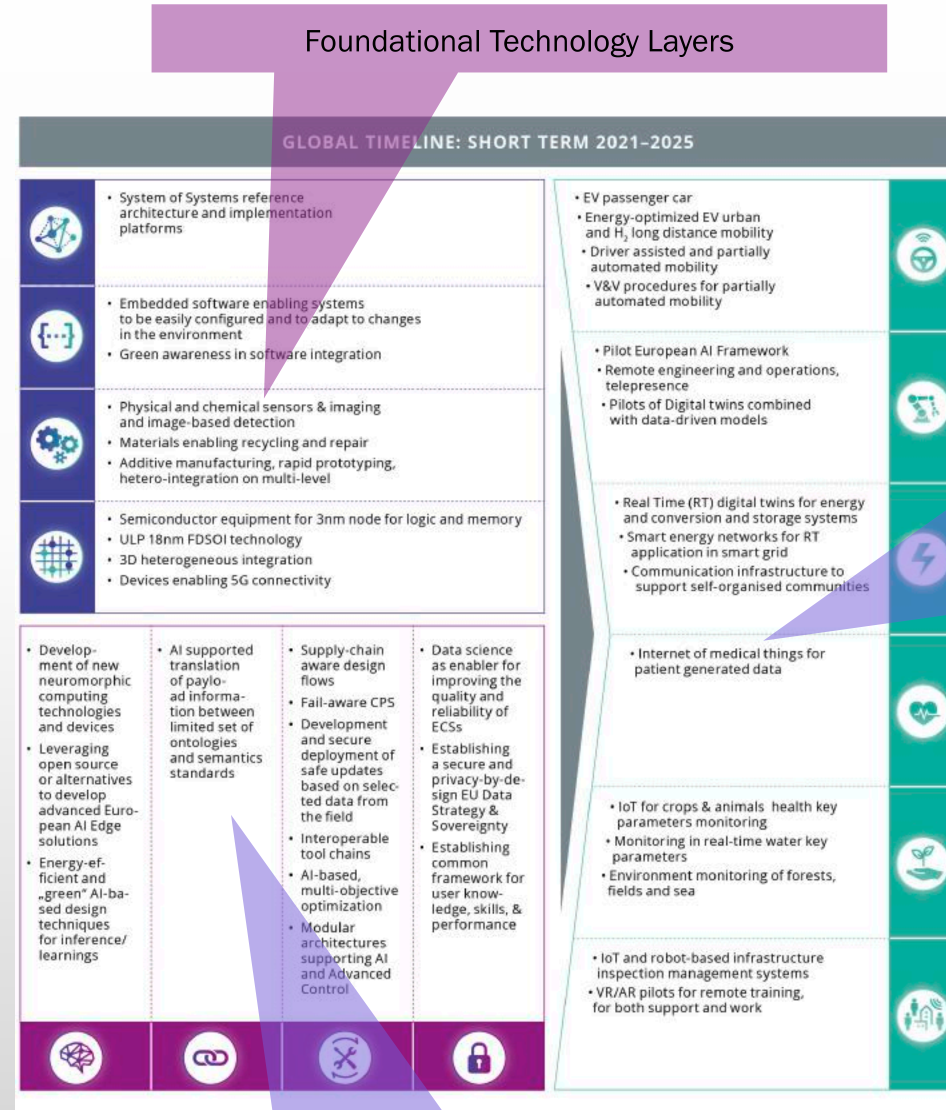
Global timelines provide a compact and structured view of the main milestones foreseen in the next 10 years.

Three period:

- Short term (2021–2025):
  The industry has a precise idea of what must be achieved during that timeframe
- Medium term (2026–2030):
  Reasonably good knowledge of what can possibly be achieved
- Long term (2031 and beyond):
  Expected achievements are more of a prospective nature

Described features expected to be available as ECS at TRL levels 8–9 (prototype or early commercialisation) within that timeframe

Detailed timelines available in each technology or application section



Cross-sectional technologies

Key Application Areas

Main web structure

ECS — *Strategic Research and Innovation Agenda 2023*

Home ECSSRIA Outline ECS SRIA Contributors Download Change History Search

Introduction and overview
Outline
1. Foundational Technology Layers
1.1 Process Technology, Equipment, Materials And Manufacturing
1.2 Components, Modules and Systems Integration
1.3 Embedded Software and Beyond
1.4 System of Systems
2. Cross-Sectional Technologies
3. ECS Key Application Areas
4. Long-Term Vision
5 Appendix A
6. Appendix B
Keywords Index

1 FOUNDATIONAL TECHNOLOGY LAYERS

Chapter 1.1 Chapter 1.2 Chapter 1.3 Chapter 1.4

1.1

Process Technology, Equipment, Materials And Manufacturing

Semiconductor process technology, equipment, ma[…] base of the ECS value chain producing the chip and packaged chip-level building blocks for all digital applications.

Nano- and microelectronics are key to achieving digital sovereignty in Europe, and they offer a range of solutions for a green and sustainable society. If Europe wants to control the development of a digital future fitted to its citizens and their requirements, as well as its social, economic, industrial and environmental goals, it needs continuous innovation in the field of semiconductor technology.

1.1.1 Scope

The key scope of this section is to cover all process technologies, equipment and materials' research and innovation to enable CMOS compatible semiconductor chip and packaged chip manufacturing inside a cleanroom environment. This includes:

- New materials and engineered substrates to improve device performance,
- process technologies, equipment and manufacturing technology to advance integrated circuit (IC) functionality and/or systems on chips,
- packaging and integration technologies for chips, chiplets, system on a chip (SoC) and system in a package (SiP).

Clearly, the scope of this section involves synergies with other sections in this ECS-SRIA. First and foremost, the section links with Components, Modules and System Integration in Chapter 1.2. In addition, this section also links with Embedded Software and System of Systems (SoS) to allow for an integral system technology co-optimisation approach to deliver application-driven solutions. More details about the synergies with other sections are described in Sub-section 1.1.6.

PROCESS, EQUIPMENT, MATERIALS AND MANUFACTURING OTHER CHAPTERS ECS KEY APPLICATION AREAS

SRIA chapters

SRIA main part

Layout entirely based on collapsible and expandable items for an improved reading experience

SRIA table of contents, which follows you while scrolling

Scope, motivations and benefits

Introduction and overview
Outline
1. Foundational Technology Layers
1.1 Process Technology, Equipment, Materials And Manufacturing
1.2 Components, Modules and Systems Integration
1.3 Embedded Software and Beyond
1.4 System of Systems
2. Cross-Sectional Technologies
3. ECS Key Application Areas
4. Long-Term Vision
5 Appendix A
6. Appendix B
Keywords Index

1 FOUNDATIONAL TECHNOLOGY LAYERS

Chapter 1.1 Chapter 1.2 Chapter 1.3 Chapter 1.4

1.1

Process Technology, Equipment, Materials And Manufacturing

Semiconductor process technology, equipment, materials and manufacturing form the base of the ECS value chain producing the chip and packaged chip-level building blocks for all digital applications.

Nano- and microelectronics are key to achieving digital sovereignty in Europe, and they offer a range of solutions for a green and sustainable society. If Europe wants to control the development of a digital future fitted to its citizens and their requirements, as well as its social, economic, industrial and environmental goals, it needs continuous innovation in the field of semiconductor technology.

1.1.1 Scope

The key scope of this section is to cover all process technologies, equipment and materials' research and innovation to enable CMOS compatible semiconductor chip and packaged chip manufacturing inside a cleanroom environment. This includes:

- New materials and engineered substrates to improve device performance,
- process technologies, equipment and manufacturing technology to advance integrated circuit (IC) functionality and/or systems on chips,
- packaging and integration technologies for chips, chiplets, system on a chip (SoC) and system in a package (SiP).

Clearly, the scope of this section involves synergies with other sections in this ECS-SRIA. First and foremost, the section links with Components, Modules and System Integration in Chapter 1.2. In addition, this section also links with Embedded Software and System of Systems (SoS) to allow for an integral system technology co-optimisation approach to deliver application-driven solutions. More details about the synergies with other sections are described in Sub-section 1.1.6.

PROCESS, EQUIPMENT, MATERIALS AND MANUFACTURING | OTHER CHAPTERS | ECS KEY APPLICATION AREAS

Process Technology, Equipment, Materials and Manufacturing
CHIP | PACKAGE | BOARD SYSTEMS | SPECIAL VERSIONS
Single Chip e.g. Si | More than Moore | System on a Chip (SoC) | Packaged Single Chip | Packaged SoC | SoC and Single Chip | BOARD/LAMINATE | Packaged Devices in Board | Chip in Board | Components, Modules
Mobility | Digital Industry | Energy | Health and

1.1.2 Technology Enabled Benefits

1.1.3 Application Breakthrough

1.1.4 Strategic Advantage for the EU

What is the chapter about?

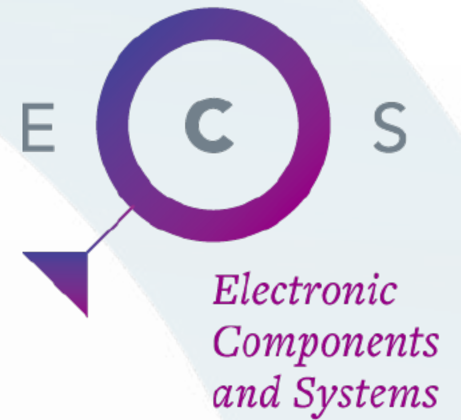
What are the societal benefits enabled by technology?

What are the applications breakthrough enabled by technology advances?

Why is it strategic for EU? What are the market figures? And the impact on the industry sector?

Major challenges (MC)

MCs are the key elements of the Open Call and Focus Topics calls



Introduction and overview
Outline
1. Foundational Technology Layers
1.1 Process Technology, Equipment, Materials And Manufacturing
1.2 Components, Modules and Systems Integration
1.3 Embedded Software and Beyond
1.4 System of Systems
2. Cross-Sectional Technologies
3. ECS Key Application Areas
4. Long-Term Vision
5 Appendix A
6. Appendix B
Keywords index

continuous innovation in the field of semiconductor technology.

1.1.1 Scope

1.1.2 Technology Enabled Benefits

1.1.3 Application Breakthrough

1.1.4 Strategic Advantage for the EU

1.1.5 Major Challenges

To achieve application breakthroughs and strategic advantage, the European position must be reinforced through leadership in all relevant equipment, materials, processes and manufacturing technologies by driving the following Major Challenges:

- **Major Challenge 1:** Advanced computing, memory and in-memory computing concepts.
  Materials and substrates, process modules and integration technology for novel devices and circuits for advanced computing, memory and in-memory computing concepts based on nano-electronic, photonic or quantum technology.
- **Major Challenge 2:** Novel devices and circuits that enable advanced functionality.
  Materials, process modules and integration technology for novel devices and circuits that enable advanced functionality (sensing, actuating, power, connectivity, biomedical, cryogenic operation, etc.).
- **Major Challenge 3:** Advanced heterogeneous integration and packaging solutions.
  Advanced heterogeneous integration and packaging solutions for system on a chip (SoC), 2.5 and 3D stacking (including chiplet technology), and smart SiP, sensor integration, photonics, power electronics, and other functionalities required for application domains (such as augmented reality/virtual reality (AR/VR), automotive, (bio)chemical, biomedical, aerospace, etc.)
- **Major Challenge 4:** World-leading and sustainable semiconductor manufacturing equipment and technologies.
  World-leading and sustainable semiconductor manufacturing equipment and technologies for the realisation of sub-2 nm node logic and memory according to PPAC roadmap requirements, chips/chiplets with single and/or multi-node layers, advanced functionality devices and heterogeneous integration technology options, as described under Major Challenges 1–3.

Major Challenge 1 | Major Challenge 2 | Major Challenge 3 | Major Challenge 4

1.1.5.1 Major Challenge 1: Advanced computing, memory and in-memory computing concepts

Semiconductor process technology and integration actions will focus on the introduction of new materials, devices and concepts, in close collaboration with the equipment, materials, modelling/simulation and embedded software communities, to allow for the necessary diversity in computing infrastructure. The applications range from high-performance cloud/edge computing in servers, office/home computing, mobile computing, and ultra-low power data processing at the IoT node level up to the highest possible performance.

1.1.5.1.1 State of the art

1.1.5.1.2 Vision & Expected outcome

1.1.5.1.3 Keyfocus

1.1.6 Timeline

1.1.7 Synergy with other themes

1.1.8 References

What are the MCs and key focus areas the project should address?

MCs can be:

- purely technology driven
- derived from application-related requirements, or from societal / strategic needs (e.g., sustainability, sovereignty)

Includes: SOTA analysis, vision to tackle the MC, expected outcomes and list of MC key focus areas

Timeline and synergies

Introduction and overview
Outline
1. Foundational Technology Layers
1.1 Process Technology, Equipment, Materials And Manufacturing
1.2 Components, Modules and Systems Integration
1.3 Embedded Software and Beyond
1.4 System of Systems
2. Cross-Sectional Technologies
3. ECS Key Application Areas
4. Long-Term Vision
5 Appendix A
6. Appendix B
Keywords Index

1.1.5 Major Challenges

1.1.6 Timeline

All leading European industry and research actors should align their activities with international roadmaps and timelines. Roadmap exercises are being conducted in various projects and communities, including NEREID[47] and the IEEE's IRDS[29], in which European academia, RTOs and industry are participating. For system integration, the International Electronics Manufacturing Initiative (iNEMI)[18] and the new Heterogeneous Integration Roadmap activities are also considered. The European R&D priorities are planned in synchronisation with global timeframes and developments that are under continuous adaptation. The timelines below are high-level derivatives from these global evolutions, and follow the structure of the four Major Challenges described above.

For Major Challenge 1, the roadmap for process technology and device/system integration presents relatively clear timelines, although economic factors will determine the speed of adoption in industrial manufacturing. Dedicated process technologies (e.g. low-power and high-operating temperature) will follow feature scaling with some delay, focusing on other performance indicators. Areas where the roadmaps and timelines are less clear (e.g. new computing paradigms) will be introduced at low technology readiness levels (TRLs).

For Major Challenges 2 and 3, the timeline of the implementation of new technologies largely depends on the needs and roadmaps of the systems, and will result from the interaction within application-driven projects and test-bed initiatives. The timing of new equipment and manufacturing solutions for these challenges should be derived from the schedules of the major European semiconductor manufacturers. This includes roadmaps for key future semiconductor domains, such as automotive, healthcare, safety and security, power, MEMS, image sensors, biochips, organ-on-a-chip, photonics, lighting, etc. Fast implementation and modification of these new device technologies will pave the way for the technologies of tomorrow.

First, the development of sub-2 nm solutions in terms of equipment and materials as part of Major Challenge 4 needs to be two-to-three years ahead of mass adoption, and is of critical importance to maintaining European leadership. Second, new equipment and materials solutions should be developed in line with the needs defined in the roadmaps of Major Challenges 1–3. Lastly, improving manufacturing efficiency and enhancing yield and reliability are ongoing tasks that need to be performed in accordance with the needs of the "more-Moore" and "more-than-Moore" domains. Fundamentals of "manufacturing science" will concern projects at rather low TRLs (typically 3–5), whereas implementation in pilot lines and full-scale manufacturing lines will contemplate higher TRL projects (typically 7–8). For most of the manufacturing science projects, the execution will take place in the medium- to long-term timespan, although shorter-term impact, such as improving the uptime of equipment due to PAD or the improvement of robustness of the manufacturing processes, will get due attention to enhance competitiveness.

MAJOR CHALLENGE	TOPIC	SHORT TERM (2023 – 2027)	MID TERM (2028-2032)	LONG TERM (2033 AND BEYOND)
Major challenge 1: Advanced computing, memory and in-memory computing concepts	**Topic 1.1:** Extensions of the scaled Si technology roadmaps High-performance Ultra-low power 3D integration	• N2 R&D • 2nd generation gate-all-around devices, forksheet integration • 18 nm FDSOI at technology platform integration level	• N1.5 R&D - 3rd generation of Gate-All-Around devices • CFET introduction • 12/16 nm FDSOI at technology platform integration level • 3D monolithic integration	• Sub-1 nm node logic and memory technology (nanowires, nanosheets) at process and device research level • Vertically stacked nanosheets • 3D monolithic integration • Beyond 10 nm FDSOI at technology platform integration level
	Topic 1.2: Exploration and implementation of unconventional devices based on materials beyond Si	• SiGe (high Ge) channel • Cu alternative solutions	• Ge channel • Optical interconnects • 2D materials exploration	• III-V channel • Low-thermal-budget-processing 2D materials device integration
	Topic 1.3: Novel device, circuit and systems	• Near/in-memory computing • 3D heterogeneous integration (logic/memory)	• In-memory computing • Neuromorphic computing (spiking)	• Quantum computing • Optical computing

1.1.7 Synergy with other themes

Europe needs leadership throughout the value chain – from the development of processes, materials and equipment to the production of devices, systems and solutions – and the deployment of services to leverage its strong differentiation potential and drive its competitiveness. The impact of technology choices on applications, and vice versa, is becoming very large and decisive regarding successful market adoption.

The new advanced applications that will drive the future of European economy can rise only through a tight interaction among the key foundational technology layers, with Chapter 1.1 (Process Technology, Equipment, Materials and Manufacturing) providing the basic physical components and their manufacturing technology, Chapter 1.2 (Components, Modules and System Integration) their integration technology into smart systems, Chapter 1.3 (Embedded Software and Beyond) the software and control technology and finally Chapter 1.4 (System of Systems) the methodology to design and combine Smart Systems in System of Systems that can solve all the application issues in a global way.

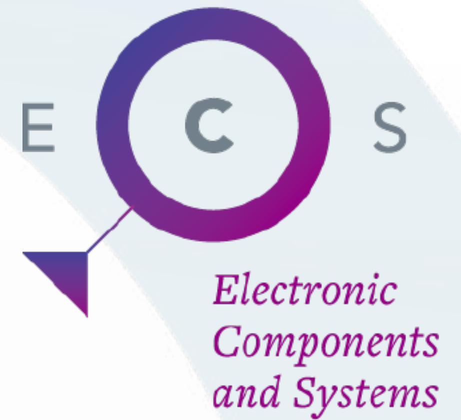
Timeline:

- MCs temporal dimension & TRL information
- Contribute to define realistic & achievable project objectives
- Help projects to stay aligned with the nature of RIA and IA

Synergies, dependencies and links with other chapters:

- Ensure the right level of projects interdisciplinarity, when needed
- Highlight other MCs to be addressed
- Link to other inspiring techs/solutions
- Link to the application level

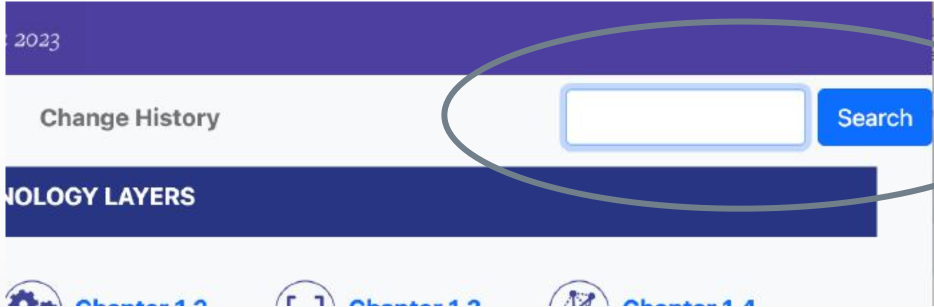
Other ECS-SRIA "Tools"



From the static "Keywords index" to the powerful Smart Search!

A

abstraction 105
accelerators 465
access control as a service (ACaaS) 442
actuating 44



Search example:

Enter your keywords:

Edge AI

Search

About searching

SEARCH RESULTS

2.1 Edge computing and embedded Artificial Intelligence

2.1 **Edge** computing and embedded Artificial Intelligence … Chapter 2.4 2.1 **Edge** computing and embedded Artificial Intelligence … and relations between the elements constituting an embedded **AI** system (figure from Gerd Teepe) The introduction of …

2. Cross-Sectional Technologies

… Chapter 2.4 2.1 **Edge** computing and embedded Artificial Intelligence … in addition tend to form a continuum between extreme **edge** , fog , mobile **edge** 95 and … and relations between the elements constituting an embedded **AI** system (figure from Gerd Teepe) The introduction of …

- Dynamic search covering the entire SRIA
- No more page numbers: only hyperlinks
- And additionally some lines of context that allow the reader to identify the most relevant area of the SRIA

ECS Collaboration Tool

A networking tool for project ideas, consortia building and partners search.

ECS COLLABORATION TOOL

ECS
COLLABORATION
TOOL

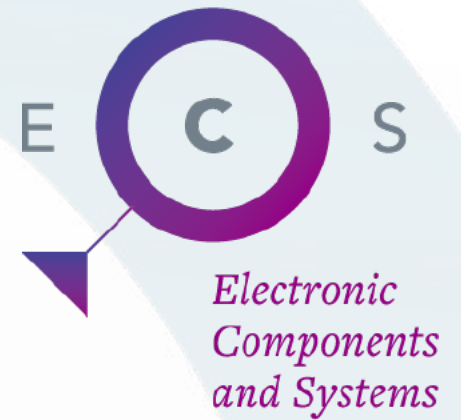
GO TO TOOL →

Electronic Components + Systems

E C S

Please, visit: https://ecscollaborationtool.eu/

ECS Collaboration Tool (2)



Create project ideas:

Initiate a project idea and invite partners, and browse other project ideas

Search for partners and build consortia:

Use the partner search to look for possible partners based on their expertise, and invite them to join your project idea

Look for other project ideas:

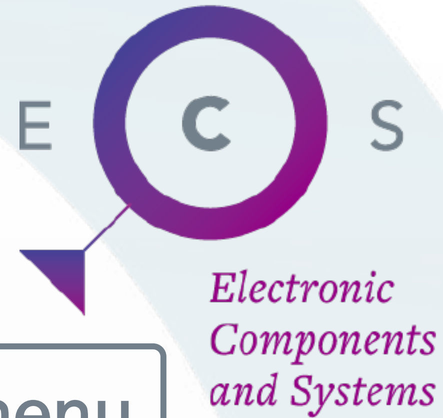
Find project ideas and send out an online request to join a consortium

Message Board - Get noticed even more:

Leave a message on the message board for possible partners or project ideas

Register and access the latest projects idea and consortia today!

ECS Collaboration Tool - Call 2023



Login & select “Ideas” in “Project ideas” option of the main menu

IDEAS

+ New idea · Message board · Download list of ideas

Ideas

Search · Reset

151 items on 19 pages

Fav	Project idea	Acronym	Contact	Organisation	Created	Keywords
☆	Canada	Spotlight on Canadian organizations attending EFECS 2022	Kasturi Narayanan	NRC-IRAP (CAN)	2022-11-07	
This is a spotlight on Canadian organizations attending EFECS 2022. Please follow the text and links below to learn more.						
☆	INDU-PACK	Inductive sintering based on micro and nano particles for microelectronic packaging	Franz Selbmann	Fraunhofer-Institut für Elektronische Nanosysteme ENAS (DEU)	2022-04-28	Packaging integration · Sintering · Chip level packaging
Title Acronym Project Description						
☆	PARY-PACK	Packaging and integration technologies for ultra-thin flexible Parylene based PCBs	Franz Selbmann	Fraunhofer-Institut für Elektronische Nanosysteme ENAS (DEU)	2022-04-28	Sensor integration · Packaging integration · Integration technologies · Parylene
Title Acronym Project Description						
☆	PRET-RISC-V	Precision Timed RISC-V CPU for Mixed Criticality Real-time Systems	Martin Kostal	Czech Technical University in Prague (CZE)	2022-01-17	Risc-v
Precision Timed RISC-V CPU for Mixed Criticality Real-time SystemsAim is to design a CPU with repeatable timing, so that it can provide WCET guarantees without over complicated WCET analysis.						

ECS SRA

Chapters

- ☐ Ch06. Systems and Components: Architecture, Design and Integration [73]
- ☐ Ch04. Digital Industry [56]
- ☐ Ch02. Health and Well-Being [54]
- ☐ Ch10. Process Technology, Equipment, Materials & Manufacturing for ECS [50]
- ☐ Ch01. Transport & Smart Mobility [44]
- ☐ Ch08. Safety, Security and Reliability [44]
- ☐ Ch03. Energy [39]
- ☐ Ch07. Connectivity and Interoperability [37]
- ☐ Ch05. Digital Life [36]
- ☐ Ch09. Computing and Storage [31]

Events

- ☐ ECS Brokerage 2023 [59]
- ☐ KDT kick-off and Brokerage 2022 [29]

To select the most recent ideas:

order by date

or select an event

IDEAS

+ New idea · Message board · Download list of ideas

Ideas

Search · Reset

59 items on 8 pages

Fav	Project idea	Acronym	Contact	Organisation	Created	Keywords
☆	test	test	Andre Hebben	Inside Industry Association (NLD)	2022-11-16	
Title Acronym Project Description						
☆	FedLCon	Fully distributed Federated Learning solution for data privacy and security	Antonio Pietrabissa	Sapienza University of Rome (ITA)	2023-01-31	Industrial cyber-physical system · Diagniostic imaging · Medical devices · Industry4.0 · Telecommunication
Title Acronym Project Description						
☆	AI beyond 5G	AI assisted communications beyond 5G	Antonio Pietrabissa	Sapienza University of Rome (ITA)	2023-01-31	AI · AI on the edge · 5g communications
Title Acronym Project Description						
☆	E-Community	Energy Communities as a mechanism for the wider adoption of clean energy technologies	José Luís Malaquias	Cleanwatts (PRT)	2023-01-31	Digital twin · Renewable energies · Energy community · Self-consumption · Digital tools

ECS SRA

Chapters

- ☐ Ch04. Digital Industry [27]
- ☐ Ch06. Systems and Components: Architecture, Design and Integration [27]
- ☐ Ch01. Transport & Smart Mobility [24]
- ☐ Ch03. Energy [24]
- ☐ Ch02. Health and Well-Being [22]
- ☐ Ch08. Safety, Security and Reliability [22]
- ☐ Ch10. Process Technology, Equipment, Materials & Manufacturing for ECS [20]
- ☐ Ch05. Digital Life [16]
- ☐ Ch07. Connectivity and Interoperability [16]
- ☐ Ch09. Computing and Storage [14]

Events

- ☑ ECS Brokerage 2023 [59]
- ☐ KDT kick-off and

ECS Collaboration Tool - Call 2023

☆ PROJECT IDEA 6: DT²

Digital Twin Tools

Short Description

Digital Twin Tools DT²
Due to the high level of complexity and heterogeneity of advanced systems it is hard to design, develop, run and maintain the Digital Twins of such systems. Different system components should be put together to make up a digital copy of a complex system. Different vendors, different standards and fast changes in architectures, technologies and components of those systems require sophisticated methods to keep the digital twins running and evolving. The objective of this project is to provide a framework to facilitate the design and development of digital twins of complex industrial systems and to provide interoperability between and within digital twins especially for heterogeneous systems. It should provide an abstraction layer to hide and to handle the complexity of building digital twins and provide more automated routines and tools. This project facilitates and speeds up the integration of digital twins into various domains especially in production systems.

Key Selling Points

What is the market relevance?
reducing the time to market
reducing the production cost
reducing the maintenance costs
What is the innovation?
New tools for creating Digital Twins
New Tools for automatic configuration of Digital Twin
What is the business impact?
more collaboration possibliites
making SMEs more competetive

Already Involved

Partners Involved
University of Luebeck
Fraunhofer
Luleau University of Technology
Institute of Computer Engineering, University of Lübeck

Looking for

Partners needed
Expertise:Partner type:SMEsLarge IndustryBattery productionUse Case providersInsurance companiesSemi Conductor industry Car industry Building automation ManufacturingUniversitiesTechnology Transfer InstitutesBlockchain developers

Countries: DE, SWE, FR,PT

Select other idea

6: DT² - Digital Twin Tools

Programme calls

- KDT-JU Call 2023

Idea presentation

ECS Brokerage 2023

This idea will be presented as poster

This idea will be presented as presentation

Digital twin · Programming tools

Request to join idea

Contact

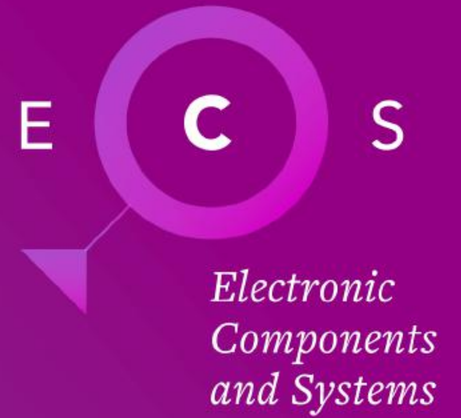
Javad Ghofrani
Institute of Computer Engineering, University of Lübeck
Germany

Uploaded documents

DT² Poster	DT² Poster
DT² Pitch Presentation	DT² Pitch Presentation

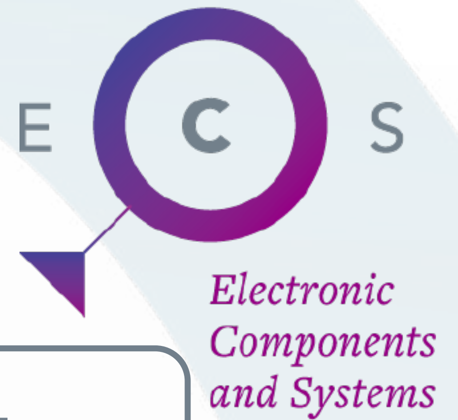
Select a project idea

- Call
- Project short description
- Coordinator contact
- Consortium
- Project idea documentation



ECS-SRIA 2023
& Focus Topics

KDT Focus Topics

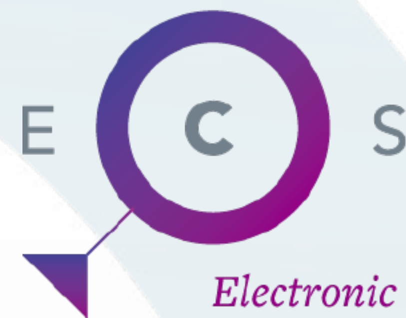


Focus Topics are topics in the ECS-SRIA that require a special attention for the sake of the Competitiveness of Europe in the ECS field and to which a specific part of the call will be dedicated to improve the coverage of the specific technology domain.

- Generally max 4 focus topics x call
- Can be RIA or IA
- Associated to a specifical call in the Work Program
- Specific budget and conditions

ECS-SRIA & Focus topics

Examples of links



6G Integrated Radio Front-End for THz Communications (Call 2023-1-IA Topic 2)

CHP 1.1 process technology, equipment, ...

- MC 2 (novel devices and circuits that enable ...) semiconductor technologies targeting THz connectivity (III-V on Si, FD SOI, RF SOI, advanced BiCMOS)
- MC 3 (advanced heterogeneous integration and packaging solutions) advanced interconnect, encapsulation, packaging for THz; 2D, 2.5D and/or 3D integration for THz

CHP 2.2 Connectivity

- MC 1 (strengthening the EU connectivity technology portfolio ...)
  - Semicon. techs like CHP1.1 MC 2
  - Ultra-low power transceivers
  - Antenna and packages for THz, on-chip antennas
  - Meta-materials for antennas, meta-materials for intelligent reflective surfaces and meta-surfaces
- MC 2 (investigate innovative connectivity technology ...)
  - New spectrum (e.g. THz) exploration

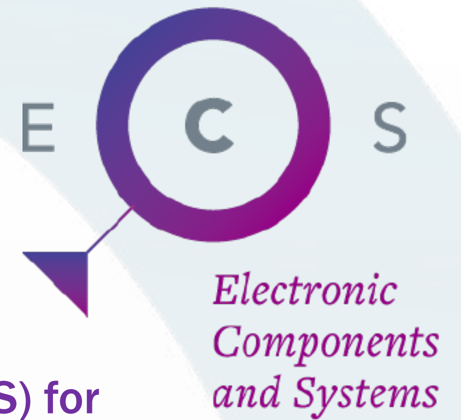
Integration of trustworthy Edge AI technologies in complex heterogeneous components and systems (Call 2023-1-IA Topic 3)

CHP 2.1 - Edge computing & embedded AI

- MC 2 (Managing the increasing complexity of systems)
  - End-2-end AI architecture including the continuum of AI-based solutions
  - Collaborative AI, transfer and meta learning
- MC-3 (supporting the increasing lifespan of devices and systems)
  - Engineering tools supporting Edge AI lifecycle
  - Self-configurability & upgradability
- MC 4 (Ensuring European sustainability)
  - Towards edge AI trustworthiness (certifiable, interpretable, explainable AI)
  - Tightly integrated open edge AI platforms and ecosystems
  - Life cycle assessment of edge AI environmental impact

ECS-SRIA & Focus topics (2)

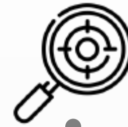
Examples of links



Hardware abstraction layer for a European Vehicle Operating System
(Call 2023-2-RIA Topic 2)

CHP 3.1 - Mobility

- MC 3 (Modular, scalable, reusable, flexible, cloud-based safe and secure end-to-end software platform able to manage software-defined mobility of the future)
  - Scalable, cloud-capable, and modular target architecture decoupling of hardware and software, and features a strong middleware layer
  - Support for current and future OSs
  - Hardware abstraction layer with open, robust, safe & secure APIs
  - Layer natively support for safety & security
  - Unified, open and shared SDK
- Indirectly contribute also to MC 4 & 5 simplifying validation and certification, and real-time data handling



Electronic Control Systems (ECS) for management & control of decentralized energy supply & storage (Call 2023-1-IA Topic 4)

CHP 3.2 - Energy

Distributed Renewable Energy Systems is linked to all challenges:

- MC 1 (Smart & Efficient - Managing Energy Generation, Conversion, and Storage Systems) smart control units; sensors, actuators, drives, controls and innovative components; Energy Management Systems; smart system integration; future of storage (including hydrogen)
- MC 2 (Energy Management from On-Site to Distribution Systems) Security, reliability and stability of total energy system; grid plug play components
- MC 3 (Future Transmission Grids) the transmission & distribution grids are the backbone of the system to monitor and control
- MC 4 (Achieving Clean, Efficient & Resilient Urban/ Regional Energy Supply) renewables sources
- MC 5 (Cross Sectional Tasks for Energy System Monitoring & Control) energy management platforms for monitoring & control

E C S

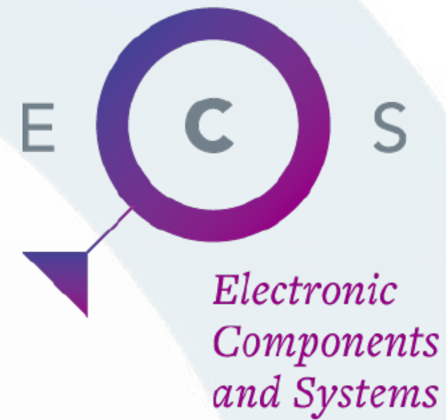
Electronic Components and Systems

ECS-SRIA 2023 Updates

For reference. For more details see also:

https://ecssria.eu/ECS-SRIA%202023%20updates%20summary.pdf

ECS-SRIA 2023 Updates



The ECS-SRIA website

Updates focused on societal benefits

Intro update with focus on climate & energy

Open Source HW and RISC-V new Appendix

4 “Main Objectives” confirmed

Structural updates

Research and market trends

New market figures

Timelines

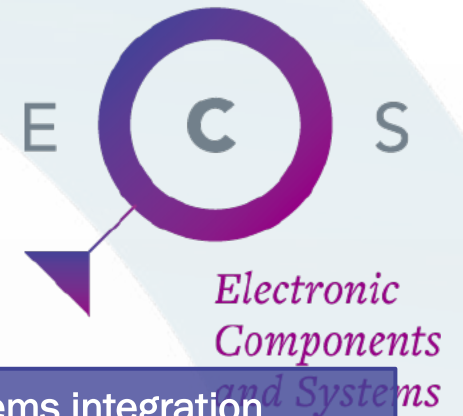
Highlight interdisciplinarity

References to recent reports and studies

Improved chapters integration & synergies

Updates focused on technology

Part 1
Foundational Technology Layers



1.1 - Process technology, equipment, materials and manufacturing

- 2D and 3D integration
- Heterogeneous integration & packaging
  - Flip Chip Ball Grid Array Substrates
  - New materials & new SiP combination diagram
- Sustainable manufacturing of chips
  - Analysis of manufacturing footprint

1.2 Components, modules & systems integration

- Review of societal benefits and application breakthroughs
- Clarified development goals and needs both from technology & functional perspectives
- Major challenges re-structured to improve clarity

1.3 - Embedded SW & beyond

- Embedded SW technologies
  - Parallelisation, SOA, SoS & new comp. par., ...
  - Heterogeneous computing architectures
- Evolvability of embedded SW
- Embedded SW architectures to enable SoS
- Reviewed the concept of Embedded Intelligence

1.4 System of systems

- SoS integration along the life cycle
  - Integration and engineering methodologies, tools and tools interoperability
- AI support to ”Trustable” SoS
- MCs Alignment with the new concepts

Part 2
Cross Sectional Technologies

2.1 - Edge computing & embedded AI

- New market figures and trends
  - Landscape of AI chips
  - Positioning of EU semiconductors industries
- New technology challenges
  - New deep learning models, automatic adaptation of complex networks, certifiable AI

2.2 - Connectivity

- Alignment with SNS on 6G
- Update of major challenge 5
  - Virtual connectivity architecture for 5G & 6G
  - Reference architecture
  - Engineering, integration and management frameworks

2.3 - Architecture and design: methods and tools

- Virtual verification & validation (V&V)
  - Support certification, simulators accuracy and faithfulness, model accuracy and faithfulness, …
- V&V of AI based systems
  - Enable V&V of AI-based functions for certification

2.4 - Quality, reliability, safety and cybersecurity

- General improvement & focus on 5G/6G
  - Improved MC1, focused on quality and reliability
  - Improved MC3, analysing the impact of 5G/6G on cybersecurity, certifications, impact of methods and tools on sustainability

Part 3
ECS Key Application Areas

3.1 - Mobility

- Key market trends, industry objectives and societal benefits
- Enabling the Software Defined Vehicle
- Towards carbon neutrality

3.2 Energy

- Evolution pace & supply needs
  - Post-pandemic effects
- New affordable technologies for sustainability
- Industrial transformation towards sustainability

3.3 Digital industry

- General review, new links to RISC-V, AI, energy, new references to recent publications

3.4 Health and wellbeing

- Improved the alignment with Health.E Lighthouse
- Synergies with Innovative Health Initiative (IHI) Joint Undertaking

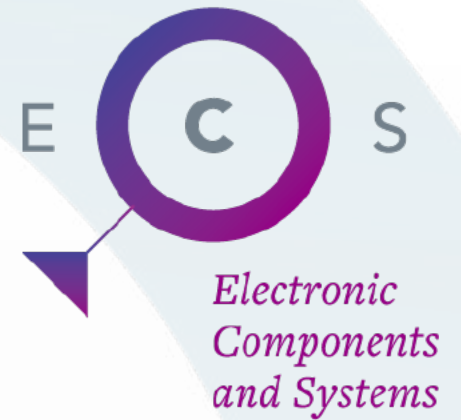
3.5 Agrifood & natural resources

- Impact of climate change
- Digital twins and block-chain
- Farming as a service
- New connectivity solutions
- Analysis of challenges

3.6 Digital society

- General review, minor changes

Part 4
Long Term Vision



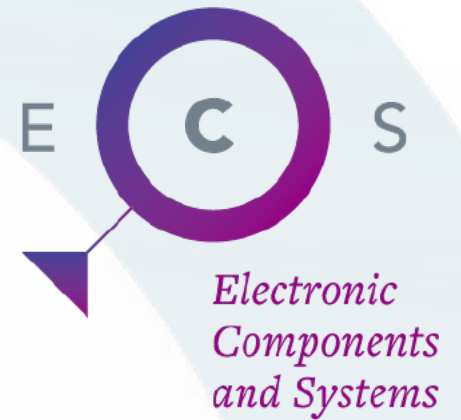
- Green Deal & sustainability objectives
  - Sustainable chips production, to reduce environmental pollution, energy and water consumption, CO_2 and GHG emission
  - ECS repair, reuse and recycle, for circular economy, non invasive and reusable electronics
- Next generation computing devices
- New frontiers in Edge AI
  - Distributed & coordinated AI
  - Social acceptance of AI
  - Explosion of diversity of ECS
- Increased heterogeneity of SoS
- Integrity of the ECS and ECS application supply chain

E C S

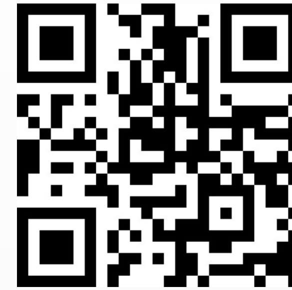
Electronic
Components
and Systems

References

References to the ECS-SRIA



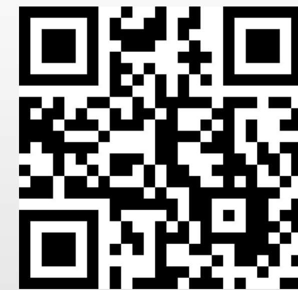
ECS-SRIA Web Site https://ecssria.eu/



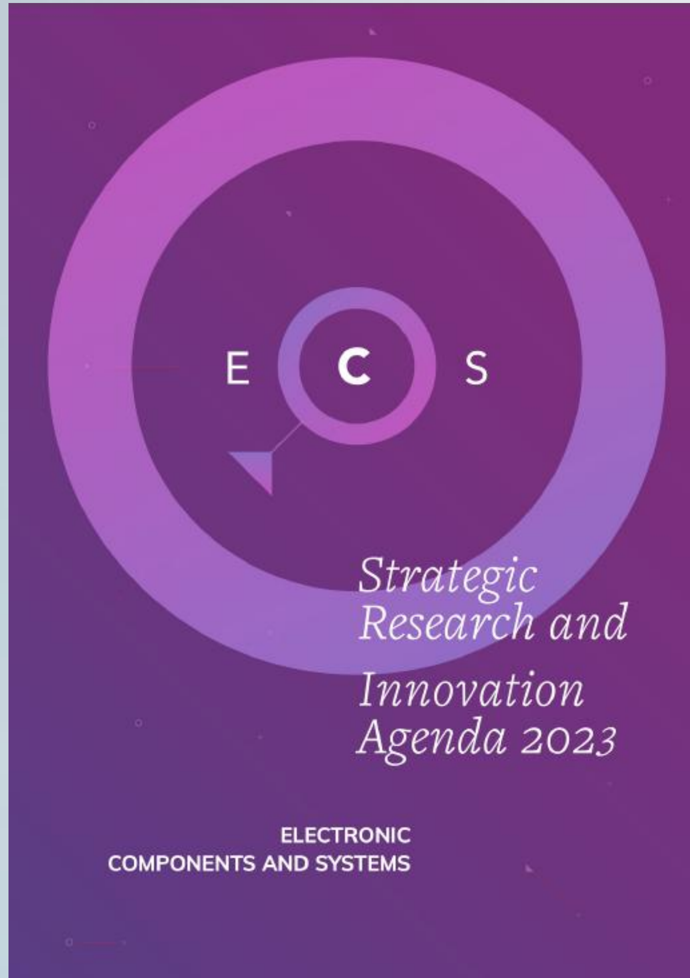
ECS-SRIA PDF Version

ECS-SRIA Outline https://ecssria.eu/download

ECS-SRIA Updates



ECS Collaboration Tool https://ecscollaborationtool.eu/



Thanks for the attention

Any question?