



ALMA MATER STUDIORUM  
UNIVERSITÀ DI BOLOGNA

# Bologna's Technopole

## The Italy/EU Computing Technology Hub

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# Bologna's Technopole

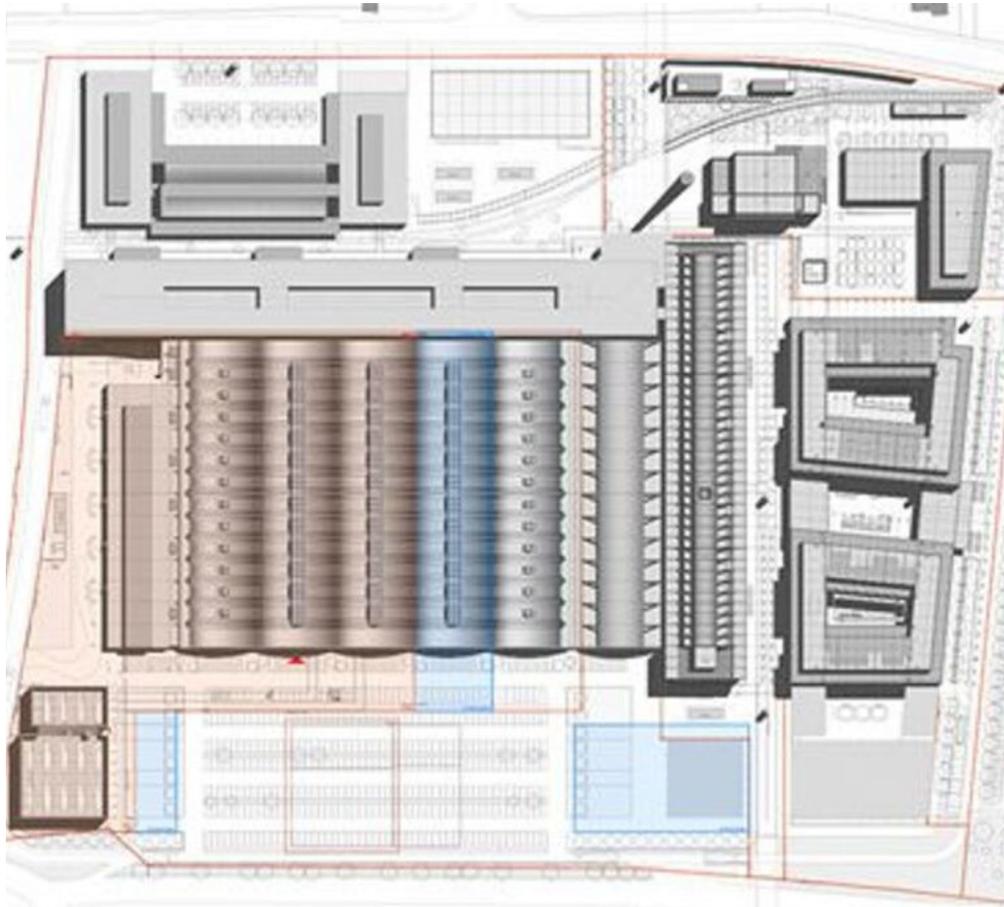


ALMA MATER STUDIORUM - UNIVERSITÀ DI BOLOGNA

IL PRESENTE MATERIALE È RISERVATO AL PERSONALE DELL'UNIVERSITÀ DI BOLOGNA E NON PUÒ ESSERE UTILIZZATO AI TERMINI DI LEGGE DA ALTRE PERSONE O PER FINI NON ISTITUZIONALI



# ECMWF Data Center





# June 1st, 2021

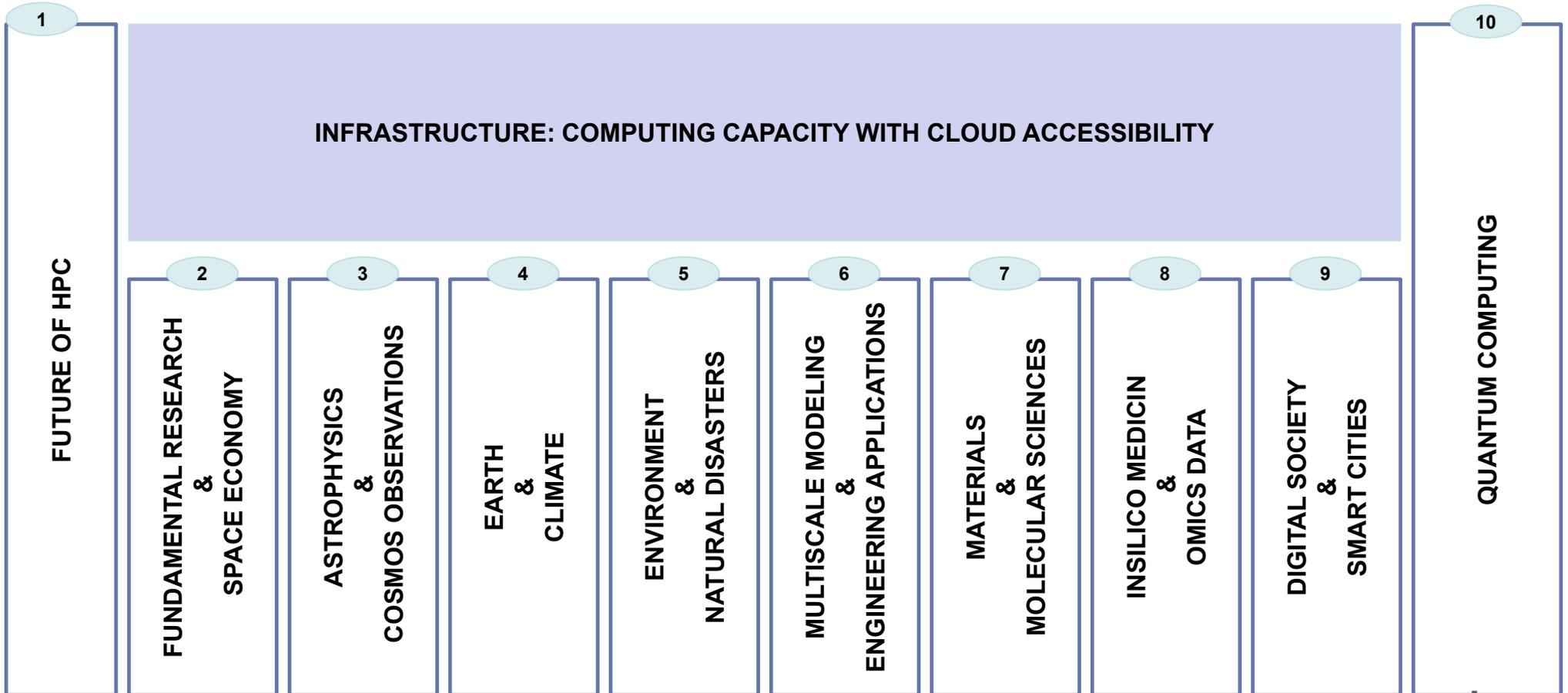


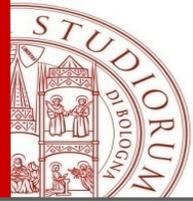
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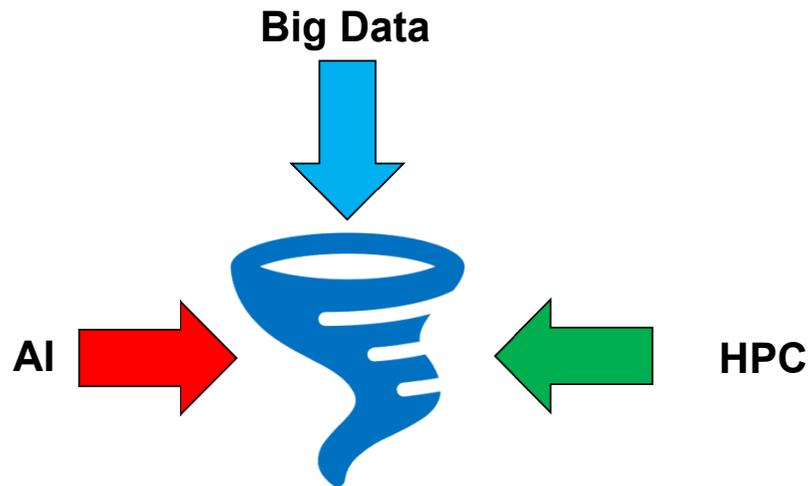


# National Center HPC, Big Data & Quantum Computing





# Convergence BD-AI-HPC... the Perfect Storm

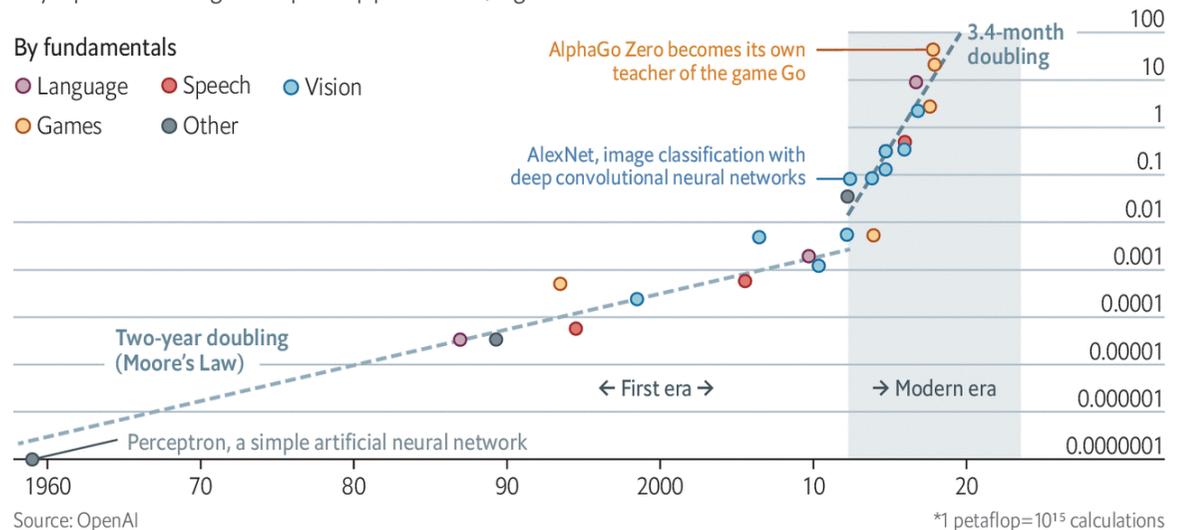


## Deep and steep

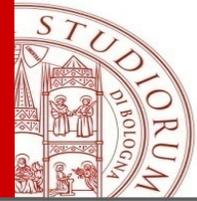
Computing power used in training AI systems  
Days spent calculating at one petaflop per second\*, log scale

By fundamentals

Language (purple dot) Speech (red dot) Vision (blue dot)  
Games (orange dot) Other (grey dot)

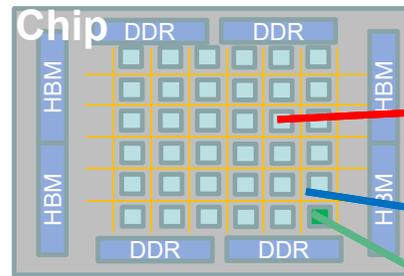


- AI as an HPC workload *drives* the evolution of HW & SW
- AI boosts «classical» HPC codes (e.g. simulations)
- Data-driven models (digital twins) using AI techniques



# HPC and digital Sovereignty: from Chips to Systems

- EU needs to re-gain control on computing!
- Technology, Architecture, Tools
- Open ISA (RISC-V), open hardware to boost innovation
- *Computing Continuum*: HPC → Cloud → Automotive → IoT Gateways → IOT edge!
- Collocation of R&D and deployment at scale → living Labs



**ARM-based processor**  
**RISC-V based accelerator**

**RHEA platform Chip**  European Processor Initiative

7(6) nm, chiplet technology

**ARM-SVE tiles** (SiPearl, ATOS)

**RISC-V power management** (UNIBO, CINECA)

**RISC-V acceleration tiles** (ETHZ, UNIBO, CEA...)

L1, L2, L3 cache subsystem + HBM + DDR



**Monte Cimone Cluster**   

6 dual-board servers, 1 Rack Unit high

RISC-V 64bit SoCs

SSD Storage, Gbit Ethernet, Infiniband interco

Ready for expansion with PCIe accelerators

**Software stack & HPC applications ported**

**Bologna's Technopole as key EU hub for Computing R&D**



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