Future Trends in Microelectronic Device Packaging

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What is “Packaging” for a Silicon Chip?

A CARRIER

- A protection
- A piece of plastics
- A thermal dissipator
- An electrical connection

A TECHNOLOGY

A PROBLEM

STI
Packaging by Assy Technology

Technology platforms:
- Organic Substrate based packages (BGA/LGA)
- Metallic Leadframe based packages
- Wafer Level Packaging
Packaging by Applications

**Sense**
MEMS and microphones (LGAs), Optical modules and Imagers towards BSI

**Power & BCD**
High dissipation, miniaturized packages (PSSO, QFNs)

**Digital with advanced CMOS**
Integration and miniaturization based on BGAs, QFPs. Towards Flip Chip & WLP
Organic Substrate - (BGA) Package

- Layout flexibility
- IO density
- Suitable for System-In-Package integration
- Electrical performance
- Compatible with wire bonding and Flip-Chip technology
Ball Grid Array - New Packages Development

Wire Bonding

Interconnection trends

Flip Chip

FCBGA/ FCTEBGA CuP

3D - adv Pack

2000-2010

Body >14²

PBGA

BGA

DCG-APG

2011-2014

FCBGA

BGA/PBGA CuWire

BGA CuWire

IBP-APG-MMS

3D, TSV, Interposer

Body <14²

BGA Std

BGA AgWire

PoP CuP

2015-2018

BGA AgWire

3D, TSV, Interposer

2.5D – 2.1 D with Stacked memory

Stacked

FC CuP, Hybrid
Stacked BGAs: basic structures

- Pyramidal structure
- Twin structure
- Film On Wire structure
Stacked BGA Evolution

3 stack 1.0mm

4 stack 1.4mm

8 stack 1.4mm

10 stack 1.6mm
Package on Package (PoP): traditional structures

Bottom Package:
- Flip chip die

Bottom Package:
- Wire bonded die

Standard size: 12x12mm
Advanced LGA SIP

- Stacked & side-by-side configuration
- Diode
- SMDs
Embedded Die

- Integration, miniaturization, shielding, short interconnections

ECP® with …

1) FCWLP
2) Stacked passive SMT
3) Stacked wirebond CSP
Embedded Capacitors

Embedded Capacitance Core
(8 um dielectric and 17 um copper)

Embedded SMDs
From BGA WB to FC or FCCP BGA

Conventional Wire Bonded BGA

Flip Chip with “solder ball” bumps

Flip Chip with “Copper Pillar” bumps
What’s 3D IC?

- 3D already exist at die or package level: wire bonding stacked dies. POP…

- 3D IC is related to interconnecting dies with high density and performance connections using TSV (Through Silicon Via) & micro bumps.
3D IC Main Technology Enablers

**Stacking**
- Process
- Accuracy

**Underfill**
- Type (Capillary, NCP…)
- Process

**Micro bumping**
- Type (Cu pillar, CuCu…)
- Pitch
- Electrical performances

**Through silicon via (TSV)**
- Type (via middle, via last…)
- Aspect ratio
- Electrical performances

**Thin wafer handling & processing**
- Temporary carrier
- Compatibility with other process
Lead Frame Packages

- Reliability
- Thermal performance
- Cost

...but limited layout flexibility (only radial signals distribution)
Leads Shape Evolution

- **straight** (‘70)
- **J bent** (‘80)
- **gull wing** (‘90)
- **no leads!** (‘00)

- **DIP**
  - Power pack.
- **PLCC, SOJ**
- **SO, TSOP, TSSOP, TQFP**
- **QFN, (BGA)**

Methods to attach IC devices to PC board
## Packaging Thickness Trend

<table>
<thead>
<tr>
<th>Values in mm</th>
<th>LQFP</th>
<th>TQFP</th>
<th>VQFPN</th>
<th>U/W/VQFN-mr</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resin</td>
<td>1.40</td>
<td>1.00</td>
<td>1.00</td>
<td>0.55/0.70/0.80</td>
</tr>
<tr>
<td>Die</td>
<td>0.375</td>
<td>0.375</td>
<td>0.280</td>
<td>0.280/0.140</td>
</tr>
<tr>
<td>Lead frame</td>
<td>0.125</td>
<td>0.125</td>
<td>0.200</td>
<td>0.100~0.125</td>
</tr>
<tr>
<td>Standoff</td>
<td>0.150 max</td>
<td>0.150 max</td>
<td>0</td>
<td>0.025-0.050</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td>1.60 max</td>
<td>1.20 max</td>
<td>1.00 max</td>
<td>0.65/0.8/1.0 max</td>
</tr>
</tbody>
</table>
QFNs Tapeless

• Tapeless QFN
  • QFN-mr (Quad Flatpack No lead – Multi Row)
  • QFN-sr (Quad Flatpack No lead – Single Row)
QFN-mr: driving forces

- L/TQFP exposed pad
- big dimensions
- thermal dissipation

- QFN-mr

- single row QFN
- pin count limited
- no leads

- BGA
- high cost & low power dissipation
- high pin count
QFN/QFN-mr: Package Characteristics

<table>
<thead>
<tr>
<th>Package Size (same I/O number)</th>
<th>BGA</th>
<th>e-TQFP</th>
<th>QFN</th>
<th>QFN-mr</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Pin Count Capability</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Warpage Excursion</td>
<td></td>
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<tr>
<td>High Frequency Capability</td>
<td></td>
<td></td>
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<tr>
<td>Thermal Dissipation</td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td>MSL &amp; SJR</td>
<td></td>
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<tr>
<td>Assembly (robust process)</td>
<td></td>
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</tr>
<tr>
<td>Testing &amp; Finishing (robust process)</td>
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</tbody>
</table>

TECHNOLOGY

<table>
<thead>
<tr>
<th>Multi row I/O Small footprint Free-routing cap.</th>
<th>Single row I/O Large footprint Mature pck</th>
<th>Single row I/O Small footprint</th>
<th>Multi row I/O Smallest footprint Flexible I/O design</th>
</tr>
</thead>
</table>

Cost & Power Dissipation

Dimensions & Lead Count

Lead Count

worst | best
Thank You!
Packaging by ST

life.augmented