Abstract—The topic of this paper is the discussion on the performance of a three-phase fault tolerant inverter with particular attention to the underrated aspect of current unbalances occurring due to the DC link voltage fluctuates after the inverter reconfiguration.

Capacitor voltage unbalance affects not only the average output voltage of the inverter, but also its performance. In fact, the inverter performance depends on the fluctuating DC-link voltage components rather than on the average DC-link voltage.

After a brief analysis of the voltage fluctuation phenomena resulting from fault tolerant configuration and their effect on load current unbalance, the Authors consider different compensating preventive or repressive strategies in different application scenarios. These strategies can operate both in open and closed loop control. The paper highlights their advantages, drawbacks and analyzes their different behavior.

Index Terms—Power electronics, Power converters, AC motor drives, fault-tolerance, Inverters.

I. INTRODUCTION.

Nowadays, reliability of power electronic converters has increased more and more over time. The progress in the field of semiconductor devices technology has allowed designers and producers to realize many complex converter structures with a very small failure rates with respect to the past. However, although less frequent, a fault event is unavoidable anyway and, sooner or later, such an event will occur.

On the other hand, many loads now present a special need for continue operation; this need is certainly greater than in the past. Not many years ago, hospitals and and a few more, were considered the only privileged loads, but actually, in a different scenario, following digital public administration, managements of large data centers with many capital sensitive information, proper conduction of business, management of a public transportation system and so on, clearly require always higher levels of reliability of the electrical power system.

This is even more important by considering that the increased level of network interconnections may imply that a failure, apparently limited to a specific area, may have a great impact, even at great distances.

In this scenario, fault tolerance of a power a system has clearly become of paramount importance. Fault tolerance is in brief the set of those features allowing different apparatuses to continue their operation with an acceptable level of performance, even in the presence of one or more faults, whenever possible and after a proper reconfiguration.

It is hard to say, in the beginning, what "acceptable level of performance" really means because this can only be defined case by case, following the systems under consideration and their particular application.

There are delicate frameworks in which a full stop of the system heavily undermines safety (e.g. the case of a submarine applications) and then clearly, in order to guarantee continuity and safety, the predefined "acceptable performance level" can not be assumed in too restrictive way.

On the contrary, in an electrical drive whose fundamental specification is the accuracy (such as in a fine positioning system), the inability to achieve this goal after a fault, must necessarily imply a lower level of fault tolerance because precision and fault tolerance are often antithetical specifications. Therefore, it may be preferable that the drive is completely stopped [1].

Although lifetime prediction is very useful in components selection stage, this design approach can not prevent from performance degradation, damages to the supplied equipments or even hazards to human life. In this way, if a fault occurs the system will handle the fault avoiding damages, at worst derating its own performances. Fault detection, handling and post-fault operation are now mandatory in modern power stages. Within inverter power stages, internal switch faults are usually classified into open-circuit or short-circuit faults.

This paper considers the problem of fault tolerance in three-phase inverter and discusses what specifically is meant by post fault "appropriate level of performance".

In the past many authors have dealt with the general problem of fault tolerant control of a VSI, focusing the main aspect in the better way to control the unfaulted power devices. In this paper, instead, the different aspect of the post fault and reconfiguration unbalance of currents is considered. Sometimes this problem has been neglected or wrongly underrated.

The load current unbalance resulting in fault tolerant mode is mainly due to voltage changes on the the DC Link capacitances. The post fault unbalance is indeed caused by the circulation of the load current on the faulty phase in the capacitors after reconnecting the faulted phase to the DC Link.
The faults of a three-phase inverter comes fundamentally from a short circuit, untimely opening, lack of control in power devices due to interruption of the drivers signals flow or to malfunction of the drivers. With this regard it should be three different behaviors can be distinguished after the fault. 

1) An open-circuit fault affects only one controllable device: The current flowing across the faulted phase can circulate only during half wave, closing its pattern through the freewheeling diode and/or the other device of the leg. The fault condition could persist long enough, causing deterioration in performance;  
2) An open-circuit fault affects an IGBT and its companion freewheeling diode: In this case, the current on the faulted phase vanishes, unless it is conducted by the remaining IGBT. The load current conduct by the healthy IGBT is highly pulsating; 
3) An entire leg of the inverter is disconnected due to the fault: This may happen if the fault occurring to one device propagates to the second device of the same leg. This is the typical case of packaged modules or that of fast fuses or another protection intervention. For damages of an entire leg, the current flowing across the faulted phase becomes zero. 

Splitting open circuit fault occurrence in the three cases is essential for the correct definition of a proper diagnosis index that does not lead to false positives enabling a prompt action. Anyway, basically a fault tolerant strategy operation consists in the following steps:  
1) diagnosis of the faulted phase;  
2) exclusion of the faulted phase;  
3) reconfiguration using auxiliary devices and restart. 

These steps should take place indeed without any one opting for an inverter shuts down. 

In the technical literature, redundant and non-redundant topologies are distinguished [4]. Redundant topologies are based on a circuital redundancy of parts of the original circuit. After fault occurrence, the redundant circuitry replaces the faulted part of the original circuit [5]–[7]. Gate drive signals of the faulted part are so connected to the redundant section neither modifying the modulation strategy nor the inverter topology. Redundant structures do not usually suffer from performance decrease at the expenses of increasing costs. As shown in Fig. 1, in non-redundant architectures a limited number of additional devices is usually required. After fault occurrence, the architecture is reconfigured by means of additional devices and the switching strategy is properly modified to accommodate the post-fault architecture [8]–[11]. 

Non-redundant topologies may suffer from performance decrease. In non-redundant topologies, after locating the fault, the corresponding phase-leg is disconnected and circuit reconfiguration will be performed by auxiliary switching devices. Circuit reconfiguration is usually realized by connecting the faulted phase pole to the midpoint of the inverter DC link by means of auxiliary switching devices. Therefore, reconfiguration usually causes a voltage unbalance on the DC link thus leading to a capacitor over-rating and increasing distortion. Furthermore, DC Link voltage unbalance also causes the appearance of an inverse current component [3], [12]. In electrical drives applications, this inverse component should be avoided because of its additional breaking torque, narrowing the motor torque range and contributing to the whole system power derating. A limitation of the DC link unbalance is then the key to improve system performances in post-fault operation. 

As already shown in the technical literature, in a fault-tolerant inverter the modulation strategy must be changed to avoid an inverse component of the load currents. In particular, the reference voltage must be significantly changed to cancel its inverse component [2]. 

In case of a fault, voltage references \( u_{ref1} \) and \( u_{ref2} \) are two sinusoidal signals controlling the healthy legs, whereas the reference of the faulty leg vanishes. Let’s assume that the corresponding complex signals are:  

\[
U_{ref1} = U_x e^{j\varphi} \quad U_{ref2} = U_x e^{-j\varphi}
\]  

(1) 

where \( U_x \) is the RMS voltage value and \( \varphi \) is the phase displacement between the signals. 

With this fundamental assumption, the magnitude of the reference voltage inverse component results: 

\[
|U_{inv(ABC)}| = \sqrt{2} U_x \sqrt{1 + \cos(\varphi \pm \frac{2\pi}{3})}
\]  

(2) 

in which the sign “+” is for a fault on the external phases A and C, while the sign “-” is for a fault on the central phase B. In both cases, for \( \varphi = \frac{2\pi}{3} = \pi \) i.e. for \( \varphi = \pm \frac{\pi}{3} \) (“+” for phase A and C and “-” for phase B) |\( U_{inv} \)| = 0. 

Unfortunately (2) has been derived by assuming a constant DC Link Voltage. The DC Link voltage is not effectively considered constant. As confirmed by both simulations and experimental results, a variable DC Link voltage produces a
residual inverse component on the load currents. Furthermore, the DC Link midpoint potential becomes unconstrained [13]. In particular Fig. 2 a) and b) show the load current pattern before and after fault and reconfiguration at 50 Hz and 5 Hz respectively. It is evident that in the case of low frequency, the unbalance of the load currents is much greater than at 50 Hz with serious consequences for the power quality in general. In the case of an electrical drive, such a current unbalance will result in a greater torque and speed ripple, especially for small inertia drives.

Fig. 3 a) show the DQO components computed in the synchronously rotating reference frame that show clearly how after fault and reconfiguration such current components can not be considered constant.

Fig. 3 b) shows the dependency of the amplitude of the D and Q components of current in the rotating reference frame versus frequency; it is noted that at low frequency the amplitude of the oscillating components is significant and can reach intolerable levels.

By using the same DQO coordinate transformation on the mathematical model of the inverter in fault tolerant mode one can obtain the following dynamical equation for the DC link voltages:

\[
3C \frac{du}{dt} = - (i_d S_q + i_q S_d) \sin (2\theta) - (i_q S_q - i_d S_o) \cos (2\theta) - \sqrt{2} i_q S_o \sin (\theta) + \sqrt{2} i_d S_o \cos (\theta) - 2 i_q S_q - 2 i_d S_d + 3 i_o
\]

\[
3C \frac{du}{dt} = - (i_d S_q + i_q S_d) \sin (2\theta) - (i_q S_q - i_d S_o) \cos (2\theta) - \left( \sqrt{2} i_q S_o - \sqrt{6} i_q \right) \sin (\theta) - \left( \sqrt{6} i_d - \sqrt{2} i_d S_o \right) \cos (\theta)
\]

\[-2 i_q S_q - 2 i_d S_d + 3 i_o
\]

where \( S_d, S_q \) and \( S_0 \) are the transformed components of the switching functions, \( i_d, i_q \) and \( i_0 \) are the current components and \( \theta = \omega t \) is the system angle. It is evident that the partial DC Link voltage will be affected by oscillating components at \( \omega \) and \( 2\omega \) angular frequency. The solution of the system (3) is not easy and can only be addressed numerically via computer simulation.

### III. Compensating Strategies.

#### A. Direct compensation.

In order to reduce voltage swinging on the DC bus, the first solution could be use of large capacitors because this naturally attenuates voltage variations, but it has drawbacks like high costs and larger sizes.
Different compensating strategies of DC link voltage fluctuations can be implemented, but, basically, they can be traced back to the modification of the reference voltage. This change, in fact, corrects the width of the individual PWM pulses for the actually operating power devices in order to correct the charging and discharging phenomena on the partial DC Link capacitors [14].

Since the current unbalance depends on voltage unbalance caused by inverse components, the problem is solved by introducing an opposite inverse component into the reference voltages to erase the existing one coming out from DC voltage swinging, so recovering performance on the load current.

It is not difficult to show that by introducing in the reference voltage a compensating term that takes the change of instantaneous voltage on the DC Link into account, the output voltages and current are properly corrected.

In more details, if $\Delta V$ is the voltage variation the partial DC Link voltages can be written as:

\[
\begin{align*}
  u_1 &= \frac{U_{DC(stiff)}}{2} + \Delta V \\
  u_2 &= \frac{U_{DC(stiff)}}{2} - \Delta V
\end{align*}
\]  

where $U_{DC(stiff)}$ is the ideal value of a stiff DC Link voltage.

By choosing the reference voltages as:

\[
v'_{ref} = \frac{u_1 + u_2}{U_{DC(stiff)}} (v_{ref} - \Delta V)
\]

where $v_{ref}$ is the uncompensated reference voltage, $v'_{ref}$ is the compensated reference voltage, the average voltage value on the load is not modified and compensation of DC voltage swinging is guaranteed.

This compensating strategy is effective, but requires the DC Link voltage measurement.

Usually the measurement of the DC Link voltage is not performed in closed loop systems and in electric drives where the reference voltages are provided by the current regulators with a compensatory term computed by the controllers themselves [15].

Figure 4 show the reference voltage for a three phase inverter directly generated by the current controllers before and after the fault. It is evident from the same Fig. 4 that the healthy leg reference voltages are not equal in magnitude and the difference is just due to the introduced compensating term. Figure 5b shows the corresponding pattern of the actual load currents (which are much more balanced than during uncompensated modulation) and the corresponding space vector trajectory that reveals to be almost circular, as it should be in the case of a triplet of balanced currents.

**B. Indirect compensation via a modified fault tolerant PWM management.**

Since the topology of a fault tolerant three-phase inverter is identical to that of a T-Type converter, it is possible to use such similarity to implement a different compensation strategy that use auxiliary bidirectional devices, Unlike traditional fault tolerant inverter, where auxiliary devices only perform the task of static breakers, new they are PWM-like controlled [16].
Figure 7: Gate drive waveforms of the reconfiguration bi-directional switches under a fault condition on leg A.

Figure 6 helps to illustrate the modified modulation strategy. In the fault-tolerant operation mode the modulating signals of the healthy legs are always 60 degrees phase shifted (thick lines in Fig. 6), whereas the one of the faulted phase is throughout null. Two biased triangular carrier signals (thin lines in Fig. 6) are compared with the modified voltage references, as in the traditional multi level modulation of a T-type inverter. The upper inverter device and the midpoint connected one are driven by comparing the modulating signals and the upper carrier. Conversely, the lower inverter switches and the midpoint connected ones are driven by comparing the modulating signals and the lower carrier. To avoid signal collisions in control of the midpoint auxiliary devices the switching pulses coming from the two different comparators are subjected to a XOR logic gate.

The auxiliary devices switching frequency equals the main switches PWM frequency. Therefore, conventional triacs are not well suited for the proposed algorithm. Bi-directional switches become here mandatory. A uniform sharing of the load current through both capacitors is due to the modulation of the auxiliary switches, thus reducing charge and discharge transients on the DC Link capacitor.

Simulation results for this compensation strategy are shown hereafter. A fault on the upper IGBT of phase A is emulated. At 0.2 s, the fault is emulated in PSIM environment by switching-off the upper IGBT of phase A. The upper IGBT will be forced in the OFF state until the end of system simulation. The diode of the upper IGBT is still correctly working. In Fig. 7 H array elements waveforms are displayed. As shown by simulation results, the fault is correctly identified and located by the detection subsystem at 0.22 s by the diagnosis algorithm [17]. The bi-directional switch of the faulted leg (A) is permanently forced to OFF state, the reconfiguration switch of the faulted leg is permanently forced to the ON state to achieve circuit reconfiguration. The bi-directional auxiliary switches of healthy legs are modulated according to the proposed fault-tolerant strategy.

In Fig. 8, load current waveforms and phase-to-neutral voltage waveforms are shown.

In Fig. 9, voltage waveforms across capacitor $C_1$ and $C_2$ of the DC link are plotted. After circuit reconfiguration, a voltage unbalance occurs on the DC Link. As shown by simulation results, under a fixed 150V DC link voltage, the peak deviation of the DC link midpoint voltage, during post-fault operation, is equal to 6 V and the transient is almost extinguished after 0.5 s after fault detection. The steady state voltage ripple is 6 V.

Simulation based on this method revealed that the fault-tolerant algorithm with PWM control of auxiliary switching devices improves performances and significantly reduces the DC link voltage unbalance by 40%.

A further benefit brought by the proposed algorithm is the reduction of the transient peak voltage.

If compared with the traditional fault-tolerant algorithm, the discussed one significantly reduces the inverse current component, even at early stage of the transient. This is of key importance in electrical drives where inverse and harmonic current components entail an unavoidable derating of the motor.
IV. CONCLUSIONS

The topic of this paper has been the discussion of the performance in a three-phase fault tolerant inverter with particular attention to load current unbalances due to the DC link voltage swinging after the inverter reconfiguration. Capacitor voltage unbalance does not only affect the average value of the synthesized inverter output voltage, but also the inverter performance in general. Indeed, the inverter performance depends on the amplitude of the low frequency DC-link voltage with respect to the average DC-link voltage. These harmonic components depend on the DC-link capacitor size, and the distortion introduced from load and grid throughout the DC-link mid-point.

Then the Authors examined the different approaches to compensation. The first strategy consists in the direct compensation of the effects of the DC link voltage swinging on the output voltage in order to bring the load currents to a condition of symmetry and balance. This strategy is very effective, but requires the direct measurement of the partial voltages on the DC link increasing the whole equipment cost, except when the system includes a closed loop current control, for which the compensating term is naturally calculated by the same current controller.

The second compensation strategy could be defined as "preventing" because it reduces the voltage fluctuations of the DC link in order to limit the resulting unbalance of the load currents to acceptable values for the correct operation of the inverter in its operating field.

This second strategy does not completely eliminate the voltage variation effects, but does not require additional voltage probes, and reduces the voltage fluctuations to the 40% of the non compensated case. This reduction significantly improves the current balance and also introduces an element of additional flexibility allowing the inverter to be controlled as a T-Type also in non fault tolerant mode.

ACKNOWLEDGMENTS

This publication was partially supported by the PON PON04a2_H "i-NEXT" Italian research program. This work was realized with the contribution of SDES (Sustainable Development and Energy Savings) Laboratory - UNINETLAB - University of Palermo.

REFERENCES


